

EE331 Digital System Design with HDL

Course Overview and Schedule

Winter 2012

Instructor - Tom Almy
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Forum -
Submit assignments to -

CATALOG DESCRIPTION

Introduces the student to a Hardware Descriptive Language and describes its role in digital design. Dataflow, Behavioral and Structural Modeling, Logic Partitioning, Hierarchical Design, CPLDs and FPGAs. DC Parameters and CPLD Timing Models. Design examples including keyboard scanner, counters, ALUs, multipliers and controllers.

Prerequisite: CST 133 or EE 133, with grade "C" or better.

PHILOSOPHY

Points mentioned in the catalog description are covered indirectly. We will spend most of the lectures learning the features of VHDL, a hardware description language that looks like a programming language but doesn't behave like a programming language. Making best use of the HDL to describe common hardware components and then building ever more complex circuits from these components will be the major thrust of the course.

It has been said "the proof is in the pudding" but I don't really know what that means! In this case the "proof" is when you can actually apply your knowledge to engineering assignments.

The early assignments, particularly the lab assignments, give detailed step-by-step instructions and involve little engineering effort. The goal is to become familiar with the tools and with VHDL. Please explore the tools and become as proficient as you can. The later labs involve increasingly more engineering effort for the student and more opportunity to be creative.

CLASS MEETINGS

We will meet on Wednesdays from January 11 through March 14 starting at 5:30 PM, sharp! We will continue until 9:50 PM with a mixture of lectures, demonstrations, and lab time. The final exam will be March 21 at 6:00PM.

Because of limited class time, students are expected to complete the reading assignment before the class. Attempt to work through the many examples provided in the text. Some of these will end up as homework assignments. The class time can

then be used to answer questions about the material, give additional examples, and offer help with the CAD tools in the lab.

Please make use of the online forums for general questions about the material throughout the week. The instructor will check the forums for posts and answer any unanswered questions several times a day.

This is the first time EE331 has been offered, and course content and timing may be changed depending on class feedback.

REQUIRED TEXT BOOK

Circuit Design and Simulation with VHDL, Second Edition, by Volnei A. Pedroni, ISBN 978-0-262-01433-5. There is a lot more information in this textbook than we will be covering in class, so don't be intimidated!

REQUIRED LAB EQUIPMENT PURCHASE

Digilent Nexys II board. Only the basic 500K gate model is necessary. The board is planned to be used in the Advanced Digital Design course and might be useful for developing your Capstone ("Senior") Project, so figure it as a long term investment. There will also be a (free) DVD provided with all reference materials from the Digilent site and the Xilinx design environment. Almost all lab work can be done at home or elsewhere with a computer that has 5 GB free disk space, 512MB (1GB preferred) RAM, an available USB port and Internet access.

READING AND HOMEWORK ASSIGNMENTS

There will be regular reading assignments from the text. Homework assignments, due in weeks where there is no lab assignment due, will cover the material presented in the text and in class. The assignments on the DVD. While the assignments can be handed in at the start of class, it is preferred if they are prepared as a Microsoft Word, Open Office, or PDF file and EMAILED to ee331@oitclass.com. Please name the file with your name and assignment, example "AlmyHomework1.pdf".

EXAMINATIONS

I consider this course to be somewhat analogous to a programming course. I've taught many of these in the past and could never figure out a decent way to have a written examination when what is important is the application of the language/tool rather than being able to recite features. So for that reason there are no examinations.

LABORATORY ASSIGNMENTS

There are five laboratory assignments. The last three assignments each count twice as much toward your final grade as the first two assignments. The lab report should consist of a roughly one page narrative of what you did that wasn't in the assignment description (I know what is in the description!), problems conquered, and critique of the project (what you learned and what still has you mystified). This

is important to show your understanding of the task and also provides me with feedback on elements that I should probably modify for future years' students. The assignments list additional material which must be turned in as part of your report. The lab reports are due as shown in the schedule, and there is a 10% grade penalty for each week or fraction thereof the report is late. The class session of March 14 is dedicated to assignment completion but might have material that wasn't fully covered in earlier weeks. Lab 5 report is due the night of the final exam, however there is a 10% bonus for turning in the Lab 5 report on March 16 or earlier. Please turn in lab reports as Microsoft Word, Open Office, or PDF files and EMAIL to. Please name the file with your name and assignment, example "AlmyLab1.pdf".

Students have asked how to handle screen captures and VHDL source code. The screen captures can be pasted directly into the document. The source code should also be included in the document (not turned in as separate files and never as an entire project folder). When you paste the source code into the document, select the code and change the font to Courier New (or similar monospaced font) with a size of 8 points.

CELL PHONES

Cell phones disrupt the class. If you have a cell phone or pager, please turn it off or have it on "vibrate" during the lecture.

STUDENT FEEDBACK

For my own benefit in improving my teaching style and in lieu of taking attendance, there will be a 30 second student feedback form to fill out at the end of each lecture. In return you will get 0.5% of the final lecture grade no matter what you say. That works out to 4.5% of the final EE 331 grade available for 5 minutes of work. What a deal! Your input as to what you like and dislike about each lecture is greatly appreciated. You will also have the opportunity to submit an anonymous question which will be answered in the forum.

GRADING

All assignments are graded based on correctness and completeness. Partial credit will be available on all questions. For essay type material in the homework and lab assignments, any spelling or grammatical errors will figure into the grade.

Component	Percentage of final grade
Lab unit 1	9%
Lab unit 2	9%
Lab unit 3	18%
Lab unit 4	18%
Lab unit 5	18%
Homework assignments	5.875% each 20% total
Feedback forms	0.5% each, 4.5% total

Numeric grades are converted to letter grades based on the chart, below.

Numeric Grade	Letter Grade
90 and up	A
at least 80, but less than 90	B
at least 70, but less than 80	C
at least 60, but less than 70	D
less than 60	F

LATE ASSIGNMENT POLICY

Homework assignments are due at 5:30 PM (the start of the class) while lab assignments are due at 9:50 PM (the end of the class) except for Lab 5 which is due at 6PM on March 21. With the exception of illness or family emergencies, late homework assignment will not be accepted. Lab assignments will not be accepted after 6PM on March 21. Missed examinations because of illness, family emergencies or job requirements (example - business trip) will be scheduled as needed.

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See assignment sheets for details

Date	Reading Due	Lecture Topic	Assignments Due
1/11		Overview	
1/18	Chapters 1,2,3 excerpts	VHDL in a nutshell	
1/25	Chapter 4 excerpts, 5	concurrent code	lab 1
2/1	chapter 6	sequential code	lab 2
2/8	chapter 7	signals and variables, counters, LED displays	homework
2/15	chapter 11	state machines	lab 3
2/22	chapter 10	simulation, memories	homework
2/29	chapter 8	package & component	lab 4
3/7	chapter 9	functions & procedures	homework
3/14	none	TBD	homework
3/21	none	none	Lab 5