

EET 361 Digital Systems I
Winter 2010
Homework Assignment 1
Due January 12

This first homework assignment will be a bit different than those that will follow because we started with basically "lab" topics.

1. Did you play the software installation video (requires Quicktime viewer)?
2. Did you install the Xilinx software?
3. Did you install the Modelsim simulator software and get the license?
4. Have you ordered a Nexys II board? Have you received it?
5. There are five classes of state machines discussed in class. How many of them are synchronous (state changes based on a clock input)?
6. Which classes of state machines have outputs that can change even if the clock input is inactive?
7. A combinational logic circuit has three inputs, a , b , and c , and one output, X . The logic equation for the circuit is $X = abc + a'bc + abc'$. Create a Karnaugh map for the circuit, and using the map realize the design using nothing but a minimal number of NAND gates and inverters. Your answer needs to show the Karnaugh map and the schematic.
8. A combinational logic circuit has three inputs, a , b , and c , and one output, X . The logic equation for the circuit is $X = abc + a'bc + abc'$. What VHDL statement will implement the logic, generating signal X from signals a , b , and c ?