

EET 361 Digital Systems I
Winter 2010
Homework Assignment 6
Due February 16

1. Do problem 16.6 in the textbook, but use only NAND gates, inverters and type D flip-flops. Don't be concerned about state assignment — you will not be graded on having the minimum logic. However you must have no greater than 8 states (no more than three state flip-flops).
2. Repeat problem 16.6, but implement as a one-hot state machine design.

Which solution took you less time? Which solution uses fewer gates? Which solution uses fewer flip-flops?