

# EET 361 Digital Systems I

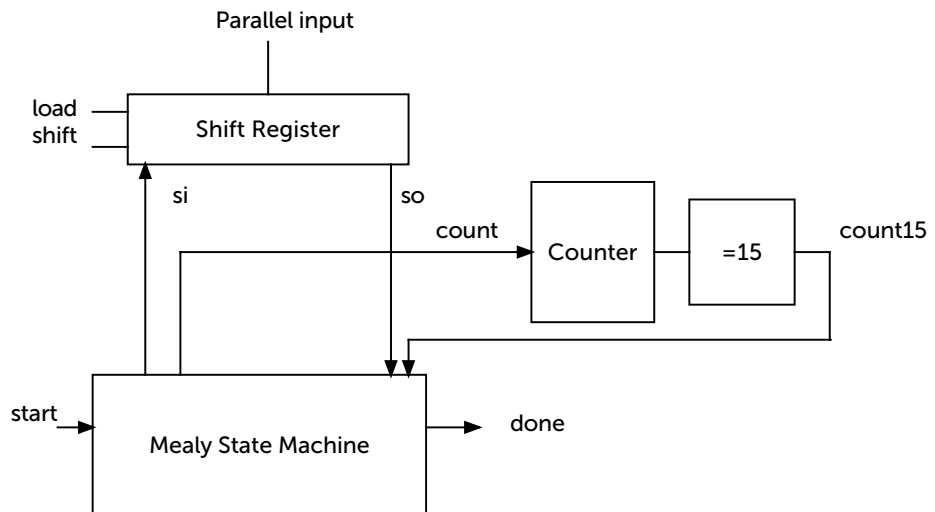
## Winter 2010

### Homework Assignment 7

Due March 2

Design a circuit to increment (add 1 to) a 16-bit shift register. This means it is a serial adder, always adding 1 to a register. You have the following components:

1. An 16 bit register with synchronous load and right-shift control inputs. The signals are named *load* and *shift* respectively. Only one of *shift* or *load* may be asserted in any clock period. The register should be loaded while in the initial (idle) state of your state machine. The serial input is named *si* and the serial output is named *so*.
2. A 4 bit counter. It counts when the signal *count* is high and is cleared when *count* is low. An output *count15* is high when the counter value is 15.
3. A Mealy State machine. It has inputs from *so*, *count15*, and *start*. It has outputs to *si*, *load*, *shift*, *count*, and *done*.



You will need to design the state machine using type D flip-flops, NAND gates, and inverters. Provide the state table or graph as well as your final state machine schematic for your solution. Use the conventional (binary encoded states) design.