

EET 361 Schedule, Winter 2010

Session	Lecture/Reading	Lab	Homework Due
1/5	Classes of state machines, Unit 10, Introduction to VHDL	Lab 1 - Digital One-Shot, Schematic-Based Design (Due 1/19)	
1/12	Unit 13, Analysis of Clocked Sequential Circuits		Assignment 1
1/19	Unit 14, Derivation of State Graphs and Tables	Lab 2 - Digital One-Shot, VHDL Design with Hierarchy (Due 2/2)	Assignment 2
1/26	Unit 17, VHDL for Sequential Logic		Assignment 3
2/2	Unit 15.1, 3, 6, 8, 9 Reduction of State Tables/ State Assignment	Lab 3 - Class 2 State Machines (Due 2/23)	Assignment 4
2/9	Unit 16 Sequential Circuit Design		Assignment 5
2/16	Unit 18, Circuits for Arithmetic Operation		Assignment 6
2/23	Unit 19, State Machine Design with SM Charts	Lab 4 - State Machine Controllers (Due 3/16)	
3/2	Unit 20, VHDL for Digital System Design		Assignment 7
3/9	Review and finish lab work		Assignment 8
3/16	Final Exam		