

EET362 Digital Systems II

Spring 2011

Week 3

Reading Assignment for April 14

Reread VHDL.PDF on RAM and ROM, the Xilinx Spartan 3 data sheet description of block ram, and if you are adventuresome, try out CoreGen for RAM generation before class.

Lecture Topics

RAMs and ROMs. We will look at generating small RAMs and ROMs in VHDL and using Xilinx CoreGen for larger memories, and using CoreGen for logic blocks.

Homework Assignment #2, Due April 21

Use CoreGen to generate a 256x8 ROM initialized so that each location contains the 1's complement of its address (address 0 contains 255, address 1 contains 254, ...). Create a module containing the ROM, and an 8 bit counter. Increment the counter with each clock period and use the counter to drive the address lines. Verify that the ROM is working correctly and has the correct values. You can do this with the following design:

