

EET362 Digital Systems II

Spring 2011

Week 6

Reading Assignment for May 5

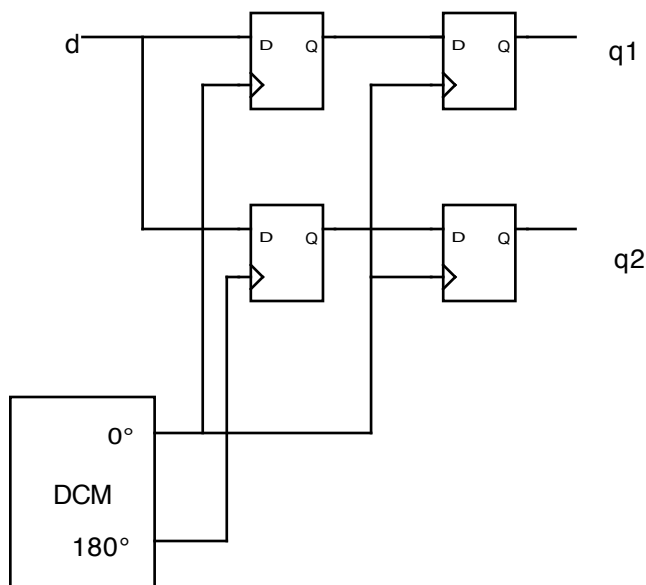
Read *Notes for Week 7* and the Xilinx documentation about the DCM.

Lecture Topics, May 5

This week we will look at source synchronous and double data rate (DDR) design techniques. We will also investigate tristate operation.

Class Exercise

1. Start with a flipflop at the top level. Add a DCM to double the clock frequency and align the phase with the input clock. Add a global constraint for a 50 MHz input clock frequency. Verify operation of the flip-flop by writing a test bench which supplies a data sequence at 100 Mb/s (megabits per second). Simulation must be post-place-and-route.
2. While the data in question 1 is arriving at “double data rate” it is only being held in a single flip flop. It is often more useful to convert the DDR data to a two bit wide data path running at the clock frequency. The circuit below accomplishes this, using the DCM to generate both clock phases. Modify your circuit from question 1 for this design and verify operation. Assign the new q2 pin and simulate post-place-and-route.



Homework Assignment #4, due May 12

In the class exercises we looked at DDR on an input pin. For this assignment you are to implement DDR on an output pin. Use the Xilinx primitive which will use the dedicated DDR logic in the output pin driver. The primitive is "ODDR2".