

EET362 Digital Systems II

Spring 2010

Course Overview

Instructor: Tom Almy

Objectives

The student will be able to design digital systems using VHDL that incorporate multiple state machines and asynchronous as well as synchronous signals. The student will be able to write simulation test benches to verify operation both functionally and with timing constraints. The student will be able to use synthesis macros (Xilinx Core Generators). The student will be able to realize the designs in FPGAs and demonstrate operation.

Class Meetings

We will meet Monday evenings, March 29 through June 7 except for Memorial Day, May 31, 5:30 to 9:50 PM. All assignments must be turned in by June 7 at 5:30 PM. There will be no final exam. The team projects will be demonstrated on June 7.

Instructor Access

Send email to xxxxxx. Please do not use my OIT address because email sent there loses its return address! My home phone is 503-692-5282, and I am available Tuesday and Thursday evenings and on the weekends. However email is usually better.

I typically arrive between 4 and 4:30 on class nights and am available for questions until the start of classes at 5:30.

There is also a forum I have set up at xxxxxx Set up an account and post there. Also check this site regularly for class information.

I send out important information via email to all students. I use your OIT address unless you have given me an alternative.

Cell Phones

Please turn off cell phones or make them "silent" during class to avoid disturbing the class.

Required Textbook and Hardware

There is an optional textbook, *Digital Systems Design using VHDL* by Charles H. Roth, Jr. However the textbook used in EET361, *Fundamentals of Logic Design, 5th Edition*, combined with lectures and various documentation will be sufficient for most students.

The Nexys or Nexys-2 FPGA board will be needed. Order from <http://www.digilentinc.com>. There will be a DVD containing software and documentation for the course that will be provided the first session. You will need a computer with roughly 4GB free disk space and at least 512MB of RAM to run the software. Windows 2000, XP, or Vista is required.

The Course Project

In order to get the best learning experience in digital systems, the bulk of the course effort will be in a single project done by the entire class, with each student assigned a portion of the design. See the document *ProjectOverview.pdf* for a full description. Each student is to keep a dated journal of their work on the project. The journal is to be maintained in a single document file. The journal is to be submitted each week to XXXXXXX.

The complete VHDL and PDP-8 assembly language listings for the projects must be turned in June 7.

Reading and Homework Assignments

An assignment sheet for weeks 2, 3, 4, 5, 7, and 8 list the lecture topics, reading which should be completed prior to class, and the homework assignment based on that week's material which is due the following week. The assignment sheets are on the DVD and are labeled by week number.

There are a total of five homework assignments, which are due at 5:30 PM on the evening of the class. Assignments can be turned in either in class or via email. Send homework assignments to XXXXXXX

The homework assignments typically require using the Xilinx ISE and writing VHDL. In most case (unless otherwise instructed) turn in your VHDL code for your answer. This would be either a printed listing (if turned in in class) or a ZIP file containing all the VHDL files (if turned in via email). BE SURE YOUR NAME IS IN ALL THE VHDL FILES! The ZIP file should have a name that includes your name and the assignment so that all the ZIP files will be unique. For instance, my first homework assignment ZIP file would be named *almy_hwk1.zip*.

Grading

Each of the five homework assignments is worth 8% of the final grade. The lecture evaluation forms (7 weeks) are each worth 0.5% of the final grade for completion. 2% of the grade is given for turning in your running journal in weeks 2 through 9 and finals week (18% total). 38.5% of the grade for completion of your part of the class project. The grading scale is 90-100 A, 80-<90 B, 70-<80 C, 60-<70 D, <60 F.

EET362 Spring 2010 Schedule

Date	Week	Lecture Subject	Assignment Due
Mar 29, 2010	1	Project	
Apr 5, 2010	2	VHDL Exercises	
Apr 12, 2010	3	Writing test benches	Homework 1
Apr 19, 2010	4	Using Coregen	Homework 2
Apr 26, 2010	5	Xilinx FPGA Architecture	Homework 3, "Week 5"
May 3, 2010	6	Project Issues	Homework 4
May 10, 2010	7	Clocks	"Week 7"
May 17, 2010	8	DDR and Tristate	Homework 5
May 24, 2010	9	Project Issues	
May 31, 2010		Memorial Day – No class meeting	
Jun 7, 2010			Demonstration of PDP-8!

Homework assignments appear in the weekly file in the week before the homework is due. For instance, homework 1 is in file "EET362 Week 2.pdf"