EE 331 Digital Systems with HDL
Oregon Tech, Wilsonville, Winter 2014

Lab Assignment 2, due Week 4, January 28

This assignment involves adding two 4 bit numbers, producing a 5 bit product. As a starting point the files lab2_top_level.vhd and lab2_test_bench.vhd have been provided. Create a new project and incorporate those two files. Incorporate the ucf file from Lab 1, either the one created from the Nexys file or from PlanAhead. You should be able to simulate or synthesize the design which will do the assignment.

However you need to implement this assignment differently. Create a new module that implements a Full Adder. The module should use concurrent assignment statements involving only logical operators. You will find an example of a full adder on page 6 of the textbook. Replace the statement in the original lab2_top_level that does the arithmetic assignment with four instances of the full adder, properly connected. Verify operation of both the simulated and the synthesized design.

At this point, save the VHDL source files and the design summary for your lab report.

Work to this point represents 85% of the grade for the lab assignment. To get full credit, modify the design so that the GENERATE statement is used to create the four full adder instances in a loop (which executes four iterations). See example 5.5 in the textbook.

To Turn In:

1. Report discussing what you did. The report should include:
2. All VHDL files you wrote or modified.
3. Design Summaries (perhaps as separate files) for the completed design(s).