EE331 Digital System Design with HDL
Course Overview and Schedule
Winter 2013

Instructor - Tom Almy
Phone -
E-Mail -
Forum -
Submit assignments to -

CATALOG DESCRIPTION

Introduces the student to a Hardware Descriptive Language and describes its role in digital design. Dataflow, Behavioral and Structural Modeling, Logic Partitioning, Hierarchical Design, CPLDs and FPGAs. DC Parameters and CPLD Timing Models. Design examples including keyboard scanner, counters, ALUs, multipliers and controllers.
Prerequisite: CST 133 or EE 133, with grade "C" or better.

PHILOSOPHY

Points mentioned in the catalog description are covered indirectly. We will start out learning the most useful features of VHDL, a **H**ardware **D**escription **L**anguage that looks like a programming language but doesn't behave like a programming language. Making best use of the HDL to describe common hardware components and then building ever more complex circuits from these components will be the major thrust of the course. The "output" of VHDL can be either for simulation or for synthesis and we will spend time with both usages.

It has been said "the proof is in the pudding" but I don't really know what that means! In this case the "proof" is when you can actually apply your knowledge to engineering assignments.

The early assignments, all of which I classify as lab assignments, give detailed step-by-step instructions and involve little engineering effort. The goal is to become familiar with the tools and with VHDL. Please explore the tools and become as proficient as you can. The later labs involve increasingly more engineering effort for the student and more opportunity to be creative.

CLASS MEETINGS

We will meet on Wednesdays from January 9 through March 13 starting at 5:30 PM, sharp! We will continue until 9:50 PM with a mixture of lectures, demonstrations, and lab time.

Because of limited class time, students are expected to complete the reading assignment before the class. Attempt to work through the many examples provided in the text.

Students have found that using the Xilinx ISE design tool is the most challenging part of the course. This is a professional tool with many more features than we need for the assignments. Pay close attention to the examples, and make use of the time at the end of the class to experiment and ask questions.

Please make use of the online forums for general questions about the material throughout the week. The instructor will check the forums for posts and answer any unanswered questions several times a day.

REQUIRED TEXT BOOK

Circuit Design and Simulation with VHDL, Second Edition, by Volnei A. Pedroni, ISBN 978-0-262-01433-5. There is a lot more information in this textbook than we will be covering in class, so don't be intimidated!

REQUIRED LAB EQUIPMENT PURCHASE

Digilent Nexys 3 board. The board is planned to be used in the Advanced Digital Design course and might be useful for developing your Capstone ("Senior") Project, so figure it as a long term investment. There will also be a (free) DVD provided with all reference materials from the Digilent site and the Xilinx design environment. All lab work can be done at home or elsewhere with a computer that has 8-9 GB free disk space, 1 GB RAM, an available USB port, and Internet access. Windows XP through Windows 7 is required. The software currently does not work on Windows 8 systems (as far as I know).

READING AND HOMEWORK ASSIGNMENTS

There will be regular reading assignments from the text and from material provided on the DVD. There are no "homework" assignments, just "lab" assignments where you put into practice what is covered in class.

EXAMINATIONS

I consider this course to be somewhat analogous to a programming course. I've taught many of these in the past and could never figure out a decent way to have a written examination when what is important is the application of the language/tool rather than being able to recite features. So for that reason there are no examinations.

LABORATORY ASSIGNMENTS

There are eight laboratory assignments, one due in each of weeks 3 through 9 and in Finals Week. The lab report should consist of a roughly one page narrative of what you did that wasn't in the assignment description (I know what is in the description!), problems conquered, and critique of the project (what you learned and what still has you mystified). This is important to show your understanding of the task and also provides me with feedback on elements that I should probably modify for future years' students. The assignments list additional material which must be turned in as part of your report. Please turn in lab reports as Microsoft

Word, Open Office, or PDF files and EMAIL to xxxxx. Please name the file with your name and assignment, example "AlmyLab1.pdf".

Students have asked how to handle screen captures and VHDL source code. The screen captures can be pasted directly into the document. The source code should also be included in the document (not turned in as separate files and never as an entire project folder). The source code needs to have comments to aid in understanding. When you paste the source code into the document, select the code and change the font to Courier New (or similar monospaced font) with a size of 8 points.

All assignments are discussed in class on the day they are due, and must be turned in at the start of the class sessions. Manage your time carefully! While students can help each other on the assignments, each student is expected to develop and submit their own individual solution. You may also ask the instructor for advise if you are having difficulties.

Because the unexpected may happen, every students gets a virtual Late Card:

Late Card

Good for one late lab assignment being accepted up to one week late.

Limitations: Only one card per student per term. Cards not transferable. Valid only for EE331, Winter 2013, Tom Almy Instructor. May not be used on the last lab assignment. No cash value. Void where prohibited by law

Use it wisely.

CELL PHONES
Cell phones disrupt the class. If you have a cell phone or pager, please turn it off or have it on “vibrate” during the lecture.

STUDENT FEEDBACK
For my own benefit in improving my teaching style and in lieu of taking attendance, there will be a 30 second student feedback form to fill out at the end of each lecture. In return you will get 0.5% of the final lecture grade no matter what you say. That works out to 5% of the final EE 331 grade available for 5 minutes of work. What a deal! Your input as to what you like and dislike about each lecture is greatly appreciated. You will also have the opportunity to submit an anonymous question which will be answered in the forum.

GRADING

All assignments are graded based on correctness and completeness. Each lab assignment is worth 11.875% of the final grade and the feedback forms are worth a total of 5% of the final grade.

Numeric grades are converted to letter grades based on the chart, below.

Numeric Grade	Letter Grade
90 and up	A
at least 80, but less than 90	B
at least 70, but less than 80	C
at least 60, but less than 70	D
less than 60	F