EE 432 Advanced Digital Design with HDL
Spring 2013
Week 2

Lecture Topic and Reading Assignment for today
Review what you know about state machines. We will talk more about them today. Topics will be:

1. Pattern matching state machines.

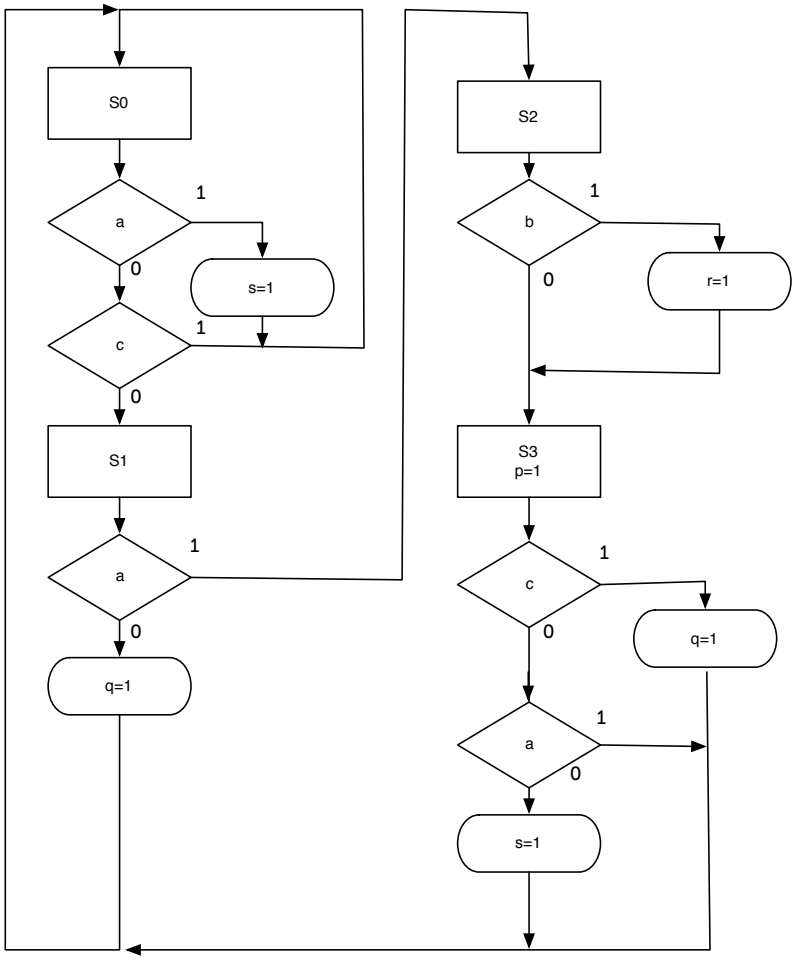
2. Controller state machines. (We have done these before!)

3. State tables, state graphs (or diagrams), ASM charts

And we will also discuss the PDP-8 as I'm sure you will have questions.

Homework Assignment #2, Due April 16 (next week)

1. Design a Moore pattern matching state machine that produces a 1 output when the preceding three bits of input have all been ones and produces a 0 output in all other cases. Show the design as a state graph. Implement the design in VHDL.
2. Implement the following ASM chart as a state machine in VHDL:



Current Project Assignment
Keep up the good work, and don't forget the journal!