EE 432 Advanced Digital Design with HDL
Spring 2013
Week 6

Lecture Topic and Reading Assignment for today
The subject for the evening is clocks and timing. We will look at the clock generating capabilities of the Xilinx part and setting timing constraints. You might want to read through the Spartan-6 Clocking Resources User Guide. We'll be investigating COREGEN's use of the DCM in class.

Some general notes are on the next page.

Homework Assignment #4, Due May 14 (next week)
Design a flip-flop and assign the D input to C4, the Q output to U16, and the clock to V10. Set a constraint for the clock period to 10 ns. Constrain the D input setup time to 5 ns. Observe whether or not the timing constraint was reached by checking the synthesizer output.

In the post place-and-route timing simulation, apply a 1000 MHz clock and apply a square wave with a period of 20.2 ns to the D input. Let the simulation run for 200 clock periods. From this determine what the actual setup time is by observing the point where the signal goes from being delayed one clock edge to being delayed two clock edges (the measurement technique works like a vernier since the data and clock frequencies differ by a small amount).

Current Project Assignment
Week 6 project deliverables due today!

Clock domains, timing

Synchronous logic – everything relates to the active clock edge (we use rising edge, but we could use falling edge or DDR – use both edges).

What are setup and hold times on inputs of flip-flops and the propagation time from clock to output?

Clock skew – shifting clock relative to data can cause timing problems – slower clock speed required, or reduce skew.

Source synchronous clocks to reduce skew problems on the board.

Xilinx clock distribution and domains.

Using DCM to reduce clock skew.

Timing constraints – you must specify the global constraints, the clock period, for any timing constraints to work. Also Pad to pad for asynchronous logic (signal passing through the part). If you have multiple clocks, you need to state how they relate. In most cases (such as the PDP-8) just the clock period will suffice.

Timing constraints at the pad must be set. Output pins – clock to pad, maximum time for data to be valid after the active clock edge. Input pins - pad to setup is the minimum setup time. Times are relative to clock net you select and clock edge. You must specify clock period for any timing constraints to work. On asynchronous inputs and outputs, these don't matter (no clock!).

Timing constraints within the chip generally not needed when using good synchronous timing design. This means no gated or derived clocks (although the DCM is handled automatically). In some cases you may have allowed for extra propagation time through large blocks of combinatorial logic by waiting two or more clock periods for the signals to propagate before latching. This will be flagged as failing the constraint unless you override. Consider a pipelined design instead.

Using the DCM to provide different clock speeds and two or four phase clocks.