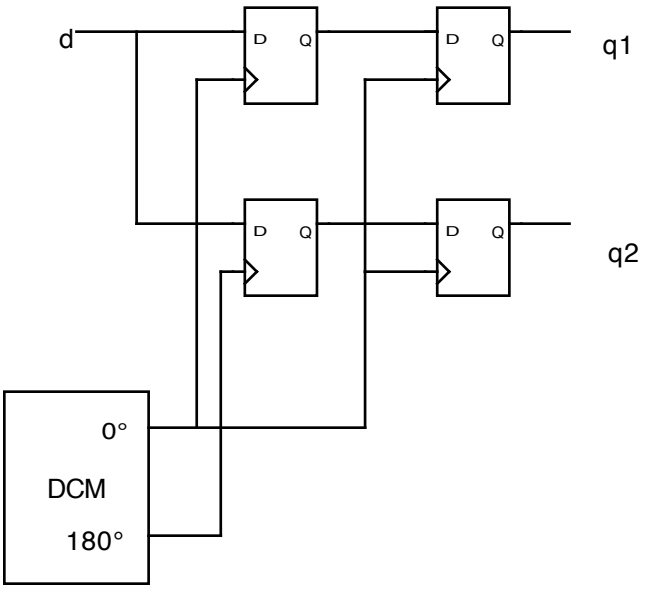
EE 432 Advanced Digital Design with HDL
Spring 2013
Week 8

Lecture Topic and Reading Assignment for today
This week we will look at source synchronous and double data rate (DDR) design techniques. We will also investigate tristate operation which you will see is surprisingly easy to do.

Class Exercise

1. Start with a flipflop at the top level. Add a DCM to double the clock frequency and align the phase with the input clock. Add a global constraint for a 100 MHz input clock frequency. Verify operation of the flip-flop by writing a test bench which supplies a data sequence at 200 Mb/s (megabits per second). Simulation must be post-place-and-route.
2. While the data in question 1 is arriving at "double data rate" it is only being held in a single flip flop. It is often more useful to convert the DDR data to a two bit wide data path running at the clock frequency. The circuit below accomplishes this, using the DCM to generate both clock phases. Modify your circuit from question 1 for this design and verify operation. Assign the new q2 pin and simulate post-place-and-route.



Homework Assignment #5, Due May 28 (next week)
In the class exercises we looked at DDR on an input pin. For this assignment you are to implement DDR on an output pin. Start with the second example above, which I will place on the forum. Use the Xilinx primitive which will use the dedicated DDR logic in the output pin driver to combine q1 and q2 into a single DDR output. The primitive is "ODDR2". You will find it in the Xilinx documentation embedded in Xilinx ISE. I'll show how to get to it in class.

Current Project Assignment
Week 8 deliverables due today.